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Sang-Kug Han [a], Hoon Choi [a], Kyo-Ho Moon [a], Young-Seok Choi [a], Sang-Hyuk Ryu [b] & Sie-Young Choi [c]

[a] Panel Department, LG Display Company Ltd., 1007, Deogeun-ri Wollong-myeon, Paju-si, Gyeonggi-do, 413-811, Korea

[b] Department of Electronics Engineering, Daegu University, Gyeongbuk, 712-714, Korea

[c] School of Electronic and Electrical Engineering, Kyungpook National University, Korea

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Capacitance Parameter Extraction and Modeling for Amorphous Silicon Thin-Film Transistors

SANG-KUG HAN,[1] HOON CHOI,[1] KYO-HO MOON,[1]
YOUNG-SEOK CHOI,[1] SANG-HYUK RYU,[2]
AND SIE-YOUNG CHOI[3,*]

[1]Panel Department, LG Display Company Ltd., 1007, Deogeun-ri Wollong-myeon, Paju-si, Gyeonggi-do, 413-811, Korea
[2]Department of Electronics Engineering, Daegu University, Gyeongbuk, 712-714, Korea
[3]School of Electronic and Electrical Engineering, Kyungpook National University, Korea

This paper presents modeling and parameter extraction of the capacitance characteristics of the inverted-staggered a-Si:H TFT in both the depletion and inversion regions of operation. The need for a model of the capacitance with variable gate-source or gate-drain bias is imperative for a robust circuit design. However, the previous model parameter expression is applied to the staggered a-Si:H TFT. In this paper, we investigated the capacitance characteristics and modeling using the new extracted method for the inverted staggered structure. The accuracy of the simulated curves using parameters extracted with the new procedure is verified with measured and calculated data.

Keywords Thin Film Transistor; a-Si:H transistor model; Kick-back Effect; Parameter Extraction; Voltage-Controlled Capacitance

Introduction

Hydrogenated amorphous silicon(a-Si:H) thin-film transistors (TFTs) are the most widely used switching devices in active matrix liquid crystal displays. AMLCDs have been applied to many information tools such as personal computers, PDAs, and picture displays. For these applications, accurate TFT models and reliable methods for parameter extraction are critical for circuit design. Shur *et al*. [1–5], Leroux, Khakzar *et al*., and other authors have presented several models for the different operational regimes of a-Si:H TFTs. They consist of the overlap capacitance (CGSO and CGDO), the oxide thickness (TOX), the dielectric constant of the oxide (EPSI) and the substrate layer (EPS) and the Zero-bias leakage current (IOL). Other parameters related to the trap distribution and intrinsic layer impurity concentration, as the Fermi level position (DEFO), the minimum density of deep states (GMIN) and the characteristic voltage for deep states (V0), can be estimated from physical ideas and procedures previously reported.

However a universal model for capacitance parameter has two problems. First, the numerical formula of the conventional capacitance parameters is applied to the staggered

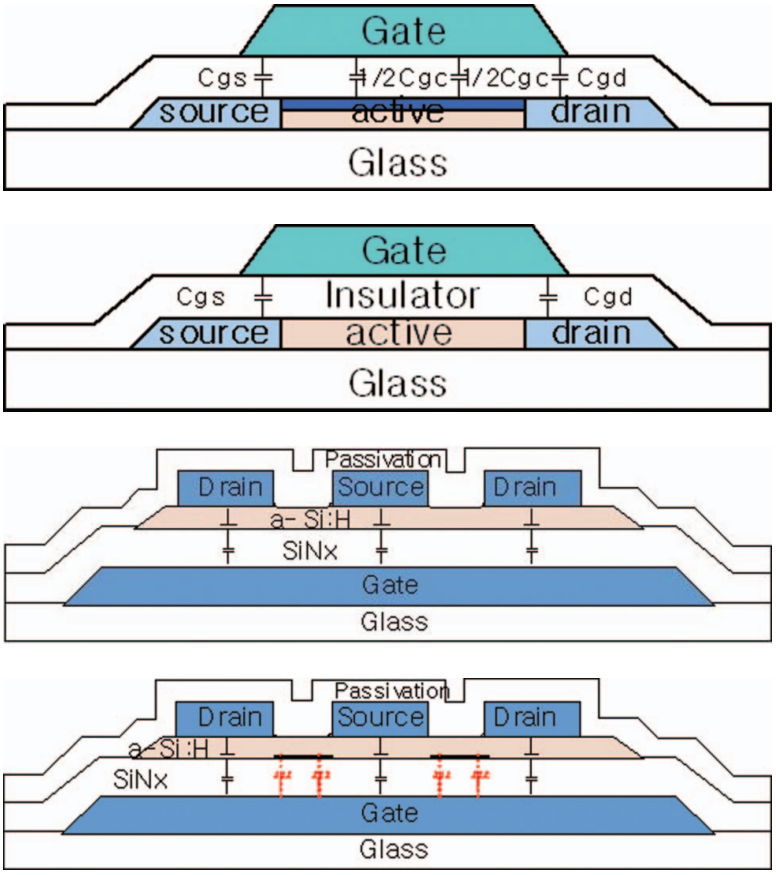
*Corresponding author.. E-mail: sychoi@ee.knu.ac.kr

and symmetric a-Si:H TFT. It is different from the inverted staggered and non-symmetric a-Si:H TFT which is the most widely employed structure. Second, there are no parameters which can control the slope and accurate value of capacitance-voltage characteristics.

In this paper, the C-V characteristics in a-Si:H TFTs with inverted staggered structures were investigated by using the AC voltage at high frequencies and moderate measurement temperatures. Also, a new method was presented to extract the capacitance parameter of these structures.

Experimental

Scheme 1 shows a cross-sectional view of (a) the staggered and (b) the inverted staggered a- Si:H TFT structure for operating voltage. These model structures were presented for the capacitance characteristics of the staggered and the inverted staggered a-Si:H TFT in both depletion and inversion regions of operating voltage.



Scheme 1. Depletion mode of the staggered a-Si:H TFT. Inversion mode of the staggered a-Si:H TFT. (a) Depletion mode of the inverted staggered a-Si:H TFT. Inversion mode of the inverted staggered a-Si:H TFT.

Figure 1 shows a physically-based, two-dimensional simulation of the inverted staggered a- Si:H TFT structure. Fig. 1 (a) shows a cross sectional view of a-Si:H for electron

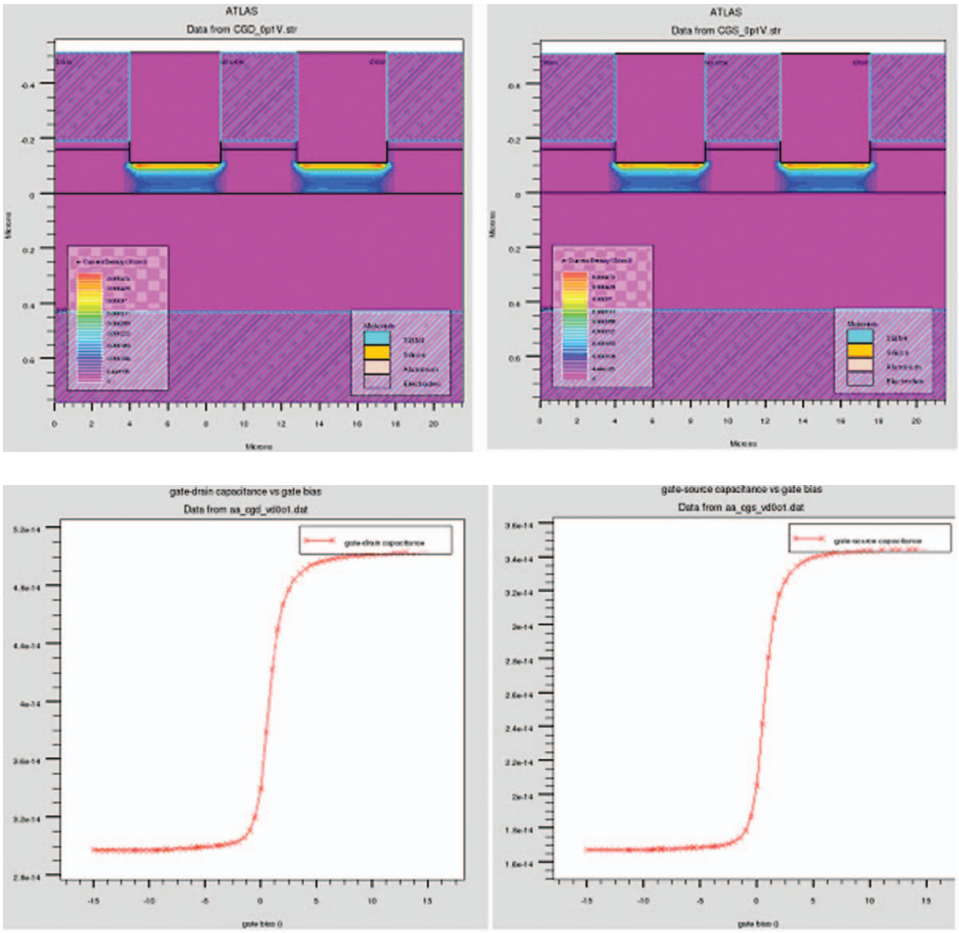


Figure 1. Physically-based, two-dimensional Simulation and of the inverted staggered a-Si:H TFT structure.

current density and (b) shows the capacitance versus voltage characteristics for amorphous silicon transistor when the gate bias is applied at 21°C and 10kHz.

Fabrication

Figure 2 shows an enlarged top view and cross sections of the inverted-staggered a-Si:H TFT used in this study. The pattern-defined channel length(L) and width(W) were 4.78 um and 30 um, respectively. The pattern-defined gate to source and gate to drain overlap areas, AreaS and AreaD, respectively, were 44 um^2 and 174 um^2. This structure was fabricated by using the following process. First, a copper gate electrode was deposited on a glass substrate by using a reactive ion sputtering and was then patterned by using standard photolithography. After that, the a-SiN:H layer, a-Si:H layer and n+ a-Si:H layers were deposited consecutively in a high- vacuum plasma enhanced chemical vapor deposition(PECVD). Thickness of the a-SiN:H, a-Si:H and n+ a-Si:H layers were 4300 Å, 1600 Å and 300 Å, respectively. The metal layer of source and drain was deposited on 3200 Å by using reactive

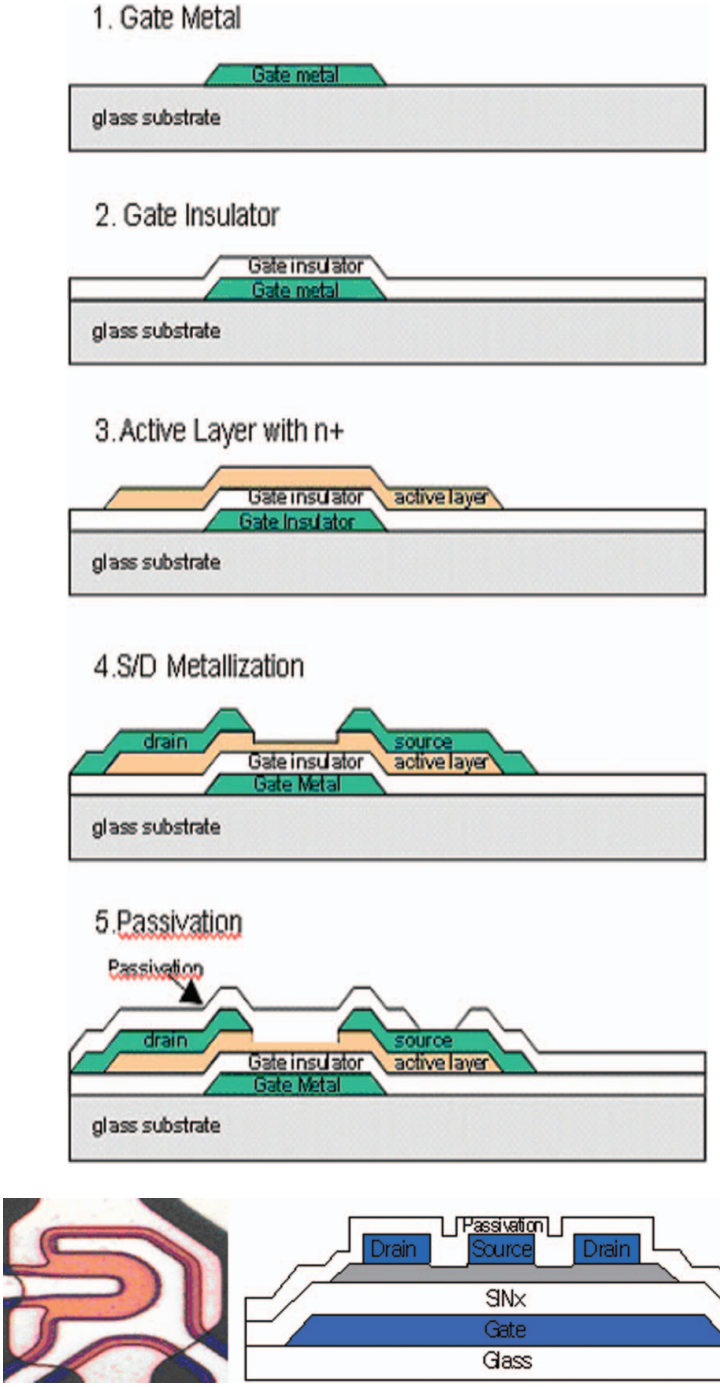


Figure 2. The process flow chart of the inverted staggered a-Si:H TFT.

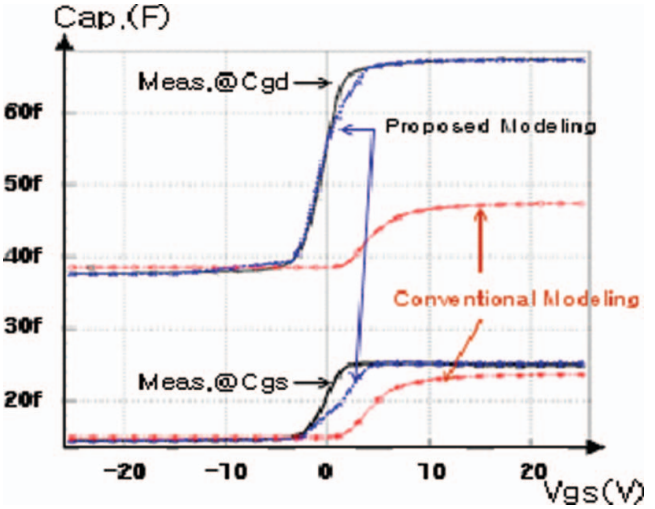


Figure 3. Measured and Simulated C-V characteristics of the inverted stagger a-Si:H TFT about the conventional and the proposed capacitance modeling at 21°C and 50 kHz.

ion sputtering. The a-Si:H, n+ a- Si:H and metals were then patterned. Finally, an a-SiNx passivation layer was deposited and patterned.

Measurements

The C-V characteristics of fabricated a-Si:H TFT were measured using an HP 4284A analyzer. Figure 3 (a) shows the variations of Cgs and Cgd without pin capacitance in both the inversion and depletion range of the gate voltage at 27°C and 50 kHz. The numerical formula of the conventional capacitance parameters was applied to the staggered and symmetric a-Si:H TFT. It is different from the inverted staggered and non symmetric a-Si:H TFT which is the most widely employed structure.

Results and Discussion

Figure 4 (a) shows the conventional and the proposed capacitance simulation results. In the depletion region, the numerical Cgd and Cgs for a universal model structure can be written as:

$$\text{Cgs\_dep\_model} = \text{CGSO} * \text{W\_effoverlap} \tag{1}$$

$$\text{CGSO} = (\text{METO} + \text{LD}) \times \frac{(\text{EPSI} \times \varepsilon_O)}{\text{TOX}} \tag{2}$$

Here CGSO is the source overlap capacitance factor(F/m), METO is the Fringe Factor, and LD is the lateral diffusion into a channel from source and drain. In addition EPSI is the relative dielectric constant of the gate insulator, and TOX is the thickness of the gate insulator. The a- Si:H permittivity wasn't reflected in this equation. Therefore, the Cgs and Cgd were increased in the depletion region. The calculated Cgs and Cgd for a conventional structure will simply be the geometric overlap capacitance. In the depletion range, Cgs and

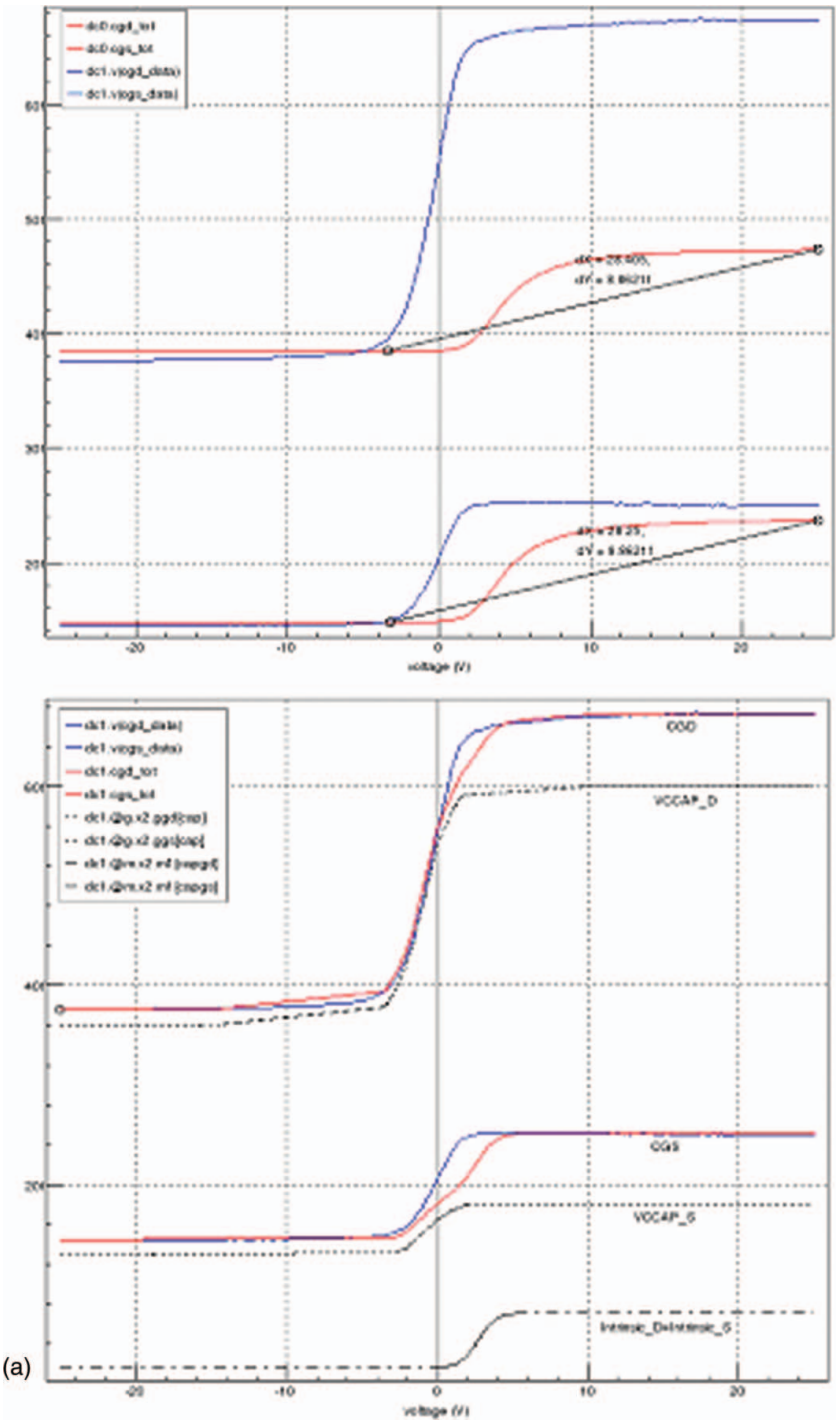


Figure 4. (a) Simulated C-V Characteristics and (b) Equivalent circuits of the conventional TFT model using geometric capacitance per unit area and the proposed TFT model using voltage controlled capacitance. *(Continued)*

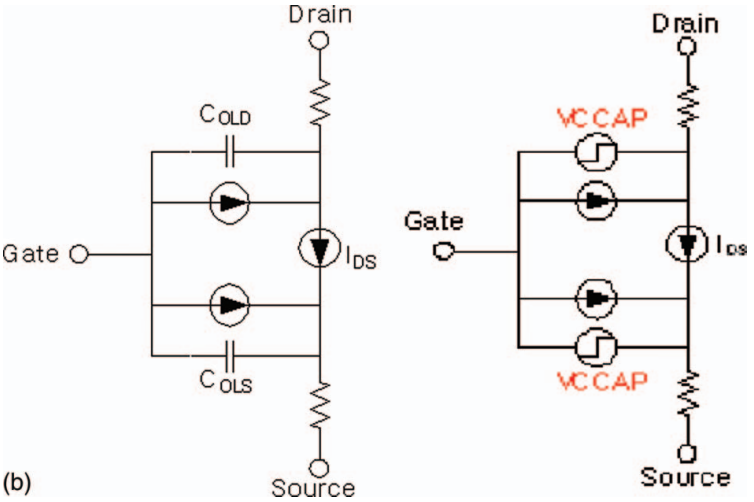


Figure 4. (Continued)

Cgd can be written as:

$$\text{Cgs-dep-cal.} = \text{Cmin} \times \text{W} \times \Delta\text{L}_\text{S} \tag{3}$$

$$\text{Cgd-dep-cal.} = \text{Cmin} \times \text{W} \times \Delta\text{L}_\text{D} \tag{4}$$

$$C_{\min} = 1/[(d_i/\varepsilon_i) + (d_{a-Si}/\varepsilon_{a-Si})] \tag{5}$$

In the inversion range, Cgs and Cgd can be written as:

$$\text{Cgs-inv.-cal} = \text{Cmax} \times \text{W} \times (\Delta\text{L}_\text{s} + \delta L_s) \tag{6}$$

$$\text{Cgd-inv.-cal} = \text{Cmax} \times \text{W} \times (\Delta\text{L}_\text{D} + \delta L_D) \tag{7}$$

$$C_{\max} = 1/[(d_i/\varepsilon_i)] \tag{8}$$

Here *di, da-Si*, εi, and ε_{a-Si} are thicknesses and the permittivity of the gate insulator and a Si:H layer. Also, δLs is the effective channel length of the source side, and δLs is the effective channel length of the drain side. That is, $\delta Ls + \delta L_D$ is equal to the channel Length L. However, the calculated data are different from the simulated data. This is because it is applied to the numerical formula of the staggered and symmetric a-Si:H TFT. That is, it is difficult to increase the capacitance accuracy in the depletion and the inversion region. To solve these problems, the capacitance characteristics of inverted staggered a-Si:H TFT were compensated using voltage-controlled capacitance when it happens the variation of the density of state(DOS). The Cgs and Cgs with voltage-controlled capacitance can be written as:

$$\text{Cgs-sim.} = \text{Cgs-vccap} + \text{Cintrinsic or Coff} \tag{9}$$

$$\text{Cgd-sim.} = \text{Cgd-vccap} + \text{Cintrinsic or Coff} \tag{10}$$

Here Cgs-vccap is the voltage-controlled capacitance for compensating Cgs-sim and Cgd-sim. Cintrinsic is the intrinsic capacitance of Cgd or Cgs in the inversion region. Coff can

Table 1. Capacitance parameter Extraction Results of the staggered and the inverted staggered a-Si:H TFT

Sample	a-Si:H TFT	
Conventional Model	**CGD0 = 1.23e-9**	**CGSO = 4.42E-10**
Proposed Model	**+CGDO = 0**	**CGSO = 0**
	+dcap1 = 36f	
	+dcap2 = 36f	
	+dcap3 = 38f	
	+dcap4 = 59f	
	+dcap5 = 60f	
	+Scap1 = 11.86f	
	+Scap2 = 13.2f	
	+scap3 = 17f	
	+scap4 = 18f	
	+AreaD = 174 AreaS = 44 W = 30.0u L = 4.78u	
	+cgdcap1 = 'Dcap1*(AreaD/174)'	
	+cgdcap2 = 'Dcap2*(AreaD/174)'	
	+cgdcap3 = 'Dcap3*(AreaD/174)'	
	+cgdcap4 = 'Dcap4*(AreaD/174)'	
	+cgdcap5 = 'Dcap5*(AreaD/174)'	
	+cgscap1 = 'Scap1*(AreaS/44)'	
	+cgscap2 = 'Scap2*(AreaS/44)'	
	+cgscap3 = 'Scap3*(AreaS/44)'	
	+cgscap4 = 'Scap4*(AreaS/44)'	
	Ggd G D1 VCCAP PWL(1) G D1 −100,'cgdcap1'	
	−15,'cgdcap2' −2.6,'cgdcap3' 0.8,'cgdcap4'	
	10,'cgdcap5' smooth = 2	
	Ggs G S VCCAP PWL(1) G S −100,'cgscap1'	
	−2.4,'cgscap2' 0.4,'cgscap3' 2,'cgscap4'	

be written as CFri.(Fringe cap.) The capacitance extraction results with voltage controlled capacitance were shown in Table 1.

Figure 5 shows the simulated results for the TFT-LCD panel at 21°C and 120Hz. This focuses specifically on the delta-Vp(ΔVp) for SXGA. The result of the UTMOST and SMARTSPICE simulators show the delta-Vp of the proposed model has been increased by 0.1362V for the conventional structure. The delta-Vo can be written as:

$$\Delta Vp = \frac{Cgs}{Cgs + Clc + Cst} \tag{11}$$

Conclusions

Although, there are many TFT devices which have been demonstrated using a-Si:H technology, it is difficult to define the accurate capacitance characteristics using the conventional model. One of the goals of this thesis is to increase the capacitance accuracy using the proposed model. The voltage controlled model has been matched by 90% for the Cgs and

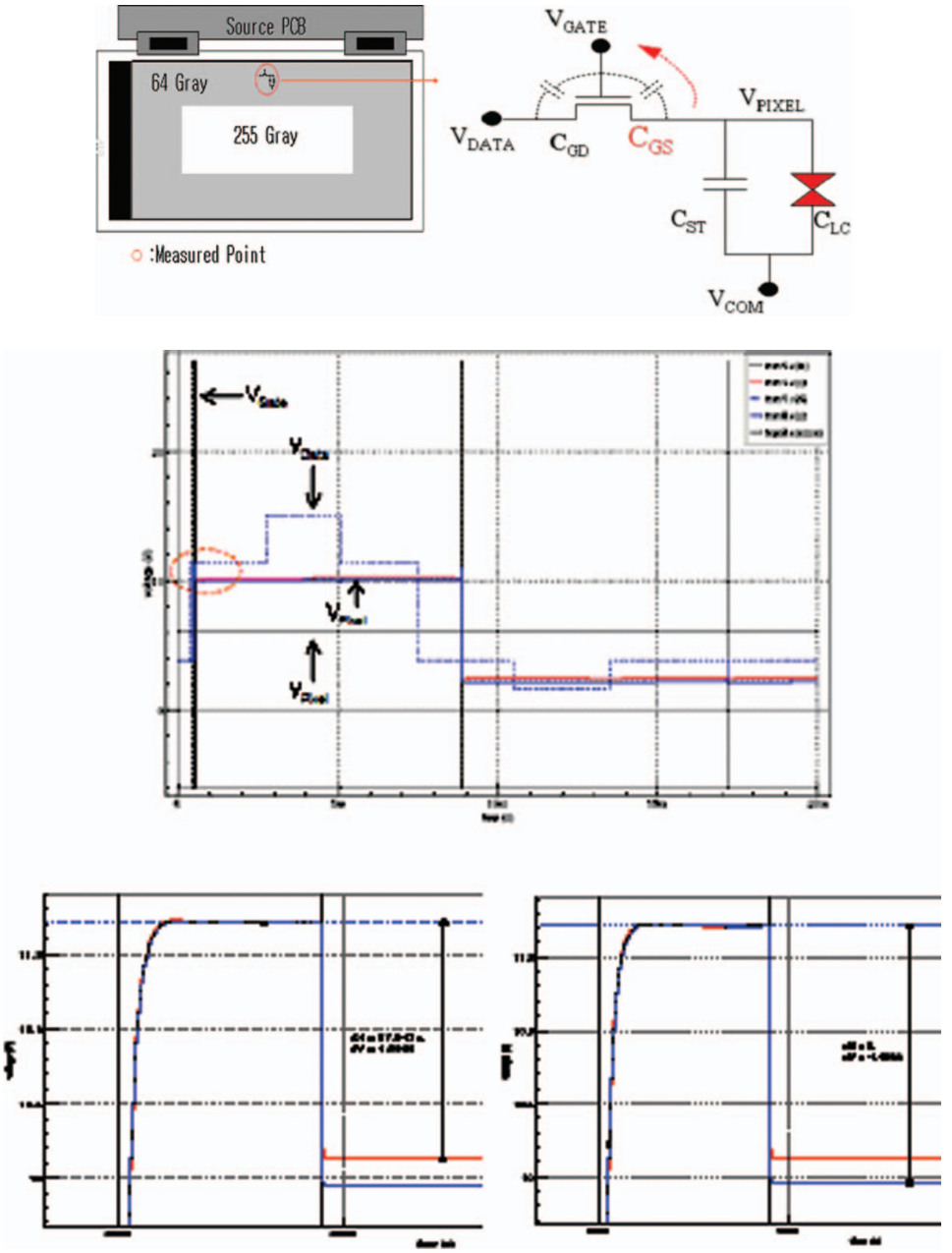


Figure 5. (a) One pixel model structure and (b) the simulated results for TFT-LCD panel at 21°C and 120 Hz. Especially, focusing on the delta-Vp(ΔVp) for SXGA.

Cgd capacitance compared to the conventional model. The simulated results for TFT-LCD are described, especially focusing on the delta-Vp (ΔVp) for SXGA. The delta-Vp for the conventional structure and the voltage controlled structure was 1.2696V and 1.4058V, respectively.

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